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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,993	10/20/2003	Ok Byung Kim	1514.1031	1374
21171	7590	10/18/2005	EXAMINER	
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			RIELLEY, ELIZABETH A	
			ART UNIT	PAPER NUMBER
			2879	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

ETV

<b>Office Action Summary</b>	<b>Application No.</b> 10/687,993	<b>Applicant(s)</b> KIM ET AL.	
	<b>Examiner</b> Elizabeth A. Rielley	<b>Art Unit</b> 2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 02 August 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-5,7,8 and 11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5,7,8 and 11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 August 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>8/23/05</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Amendment***

Amendment filed 8/2/05 has been entered and considered by the Examiner. Claims 6, 9, and 10 have been canceled. Currently, claims 1-5, 7, 8, and 11 are pending in the instant application.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 1-5, 7-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-5 and 7-8 recites the limitation "the primary crystal grain boundaries... of the second plurality of thin film transistors" in claim 1. There is insufficient antecedent basis for this limitation in the claim.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1–3, 5, 7-8, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Mitnaga et al (US 5923997)

In regard to claim 1, Mitnaga et al teach a display device with a polysilicon substrate (250; figures 3b and 5a; column 13 line 47 to column 14 line 55), comprising: a display region (PTFT, 111, 133; figure 2; column 13 line 11-column 14 line 55) and a driving region (NTFT; figure 2; column 13 line 11 – column 14 line 55; claims 10-15); a first plurality of thin film transistors in the display region (PTFT; figure 2); a second plurality of thin film transistors (NTFT) and primary crystal grain boundaries (216; figure 5B; column 14 lines 55-65) in the polysilicon substrate in the display region (claim 10); wherein the primary crystal grain boundaries are inclined to a first direction of current flowing from source (208) to drain (210) of each of the first plurality of thin film transistors at an angle of  $-30^{\circ}$  to  $30^{\circ}$  (figure 5b; column 14 line 56 to column 15 line 4). And wherein the primary crystal grain boundaries are inclined to a second direction of current flowing from source to drain of each of the second plurality of thin film transistors at an angle of  $30^{\circ}$  to  $150^{\circ}$  (claim 10; lines 47-column 16 line 17).

In regard to claim 2, Mitnaga et al ('997) teach the primary crystal grain boundaries (216) are parallel to the first direction of current (column 14 lines 48-55).

In regard to claim 3, Mitnaga et al ('997) teaches a first number of the primary crystal grain boundaries exist in active channel regions of each of the first plurality of thin film transistors (column 13 line 66 to column 14 line 12).

In regard to claim 5, the Applicant is claiming a display device including a method (i.e.: process) of making the polysilicon substrate; consequently, claim 5 is considered a “product-by-process” claim. In spite of the fact that a product-by-process claim may recite only process limitations, it is the product and not the recited process that is covered by the claim. Further, patentability of a claim to a product does not rest merely on the difference in the method by which the product is made. Rather, it is the product itself, which must be new and not obvious (see MPEP 2113). Hence, Mitnaga et al ('997) disclose of a polysilicon substrate meets the structural limitation of the claimed invention.

In regard to claim 7, Mitnaga et al ('997) teach the primary crystal grain boundaries are perpendicular to the second direction of current (column 15 line 48-column 16 line 18).

In regard to claim 8, Mitnaga et al ('997) teach second number of the primary crystal grain boundaries exist in active channel regions of each of the second plurality of thin film transistors (column 15 line 48-column 16 line 18).

In regard to claim 11, Mitnaga et al ('997) teach a display device with a polysilicon substrate comprising: a driving region (claim 13); a plurality of thin film transistors in the driving region (claim 10); and primary crystal grain boundaries in the polysilicon substrate in the driving region (claim 10); and secondary primary crystal grain boundaries in the polysilicon substrate in the driving region (claim 10); wherein the primary crystal grain boundaries are inclined to a direction of current flowing from source to drain of each of the plurality of thin film transistors at an angle of 30.degree. to 150.degree and the secondary crystal grain boundaries are substantially perpendicular to the current flowing from the source to the drain (claim 10).

*Response to Arguments*

Applicant's arguments filed 8/2/05 have been fully considered but they are not persuasive.

In regard to Applicant's argument that Mitnaga et al ('997) fails to teach a display device with a polysilicon substrate comprising: a display region and a driving region; a first plurality of thin film transistors in the display region; a second plurality of thin film transistors and primary crystal grain boundaries in the polysilicon substrate in the display region; wherein the primary crystal grain boundaries are inclined to a first direction of current flowing from source to drain of each of the first plurality of thin film transistors at an angle of  $-30^{\circ}$  to  $30^{\circ}$  wherein the primary crystal grain boundaries are inclined to a second direction of current flowing from source to drain of each of the second plurality of thin film transistors at an angle of  $30^{\circ}$  to  $150^{\circ}$ . The Examiner respectfully disagrees. In claims 10-15, Mitnaga et al teaches a display region and a driving region; a first plurality of thin film transistors in the display region; a second plurality of thin film transistors and primary crystal grain boundaries in the polysilicon substrate in the display region; wherein the primary crystal grain boundaries are inclined to a first direction of current flowing from source to drain of each of the first plurality of thin film transistors at an angle of  $-30^{\circ}$  to  $30^{\circ}$  wherein the primary crystal grain boundaries are inclined to a second direction of current flowing from source to drain of each of the second plurality of thin film transistors at an angle of  $30^{\circ}$  to  $150^{\circ}$ .

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*Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jung (US 6177301) discloses growing silicon grains orientated at a first direction, then at a second direction for a TFT.

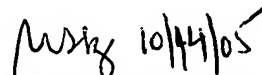
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elizabeth A. Rielley whose telephone number is 571-272-2117. The examiner can normally be reached on Monday - Friday 7:30 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar Patel can be reached on 571-272-2457. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Elizabeth Rielley

*Examiner*  
Art Unit 2879

  
MARICELI SANTIAGO  
PRIMARY EXAMINER